

# Precision Synthesis

## PRODUCT OVERVIEW



*Precision Synthesis is the industry's foremost FPGA design solution, offering ease of use, high-productivity flows and outstanding QoR within a complete vendor-independent design methodology.*

## Multi-Vendor, Physically Aware FPGA Synthesis

FPGA designs have become increasingly challenging. Incremental design methodologies are needed to effectively manage complexity, reduce risk and accelerate time to market. Moreover, it has become very important for designers to fine-tune FPGA implementations and thus ensure that their challenging designs meet technical and business requirements.

"Pushbutton-only" flows fail to provide efficient reuse and adequate implementation control to reliably meet design goals. They ultimately limit a design team's ability to consistently bring differentiated products to market.

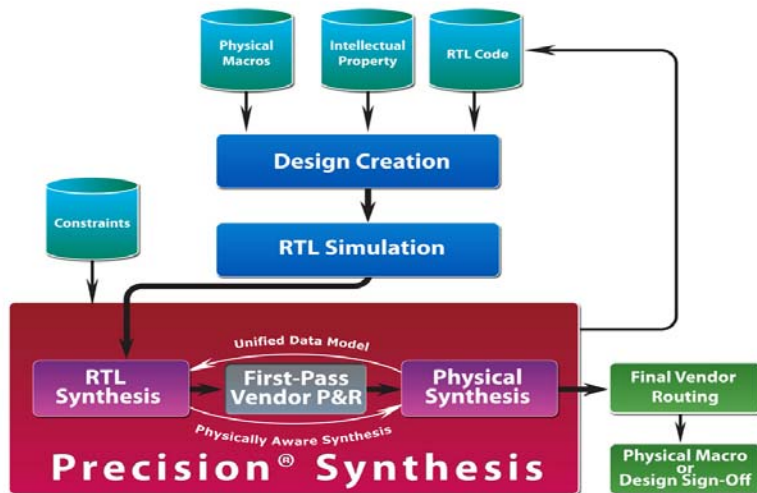
Combining out-of-the-box ease-of-use, high-productivity design flows and industry-leading quality of results (QoR), even for the most advanced FPGA devices, Precision® Synthesis provides excellent design analysis capabilities and outstanding physical implementation and timing control -- all within a truly vendor-independent design methodology.

## Start Right with Easy-to-Use RTL Synthesis

Regardless of design entry method or target architecture, RTL synthesis has always been the backbone of any FPGA design process. The quality of the netlist created by the synthesis tool sets the stage for the effort needed to meet design

## Key Product Features:

- **Integrates Powerful RTL Synthesis with Advanced Physical Optimization Flows**
- **Start Designs Right**
  - Provides superior support for Verilog 2001 and VHDL
  - Supports major FPGA vendor-generated cores
  - FPGA vendor-independent synthesis technology integrates with vendor P&R tools for excellent QoR
  - New Modular Design Flow enables efficient reuse of physically implemented components, thus leveraging previous success in future FPGA designs
- **Improve Designs Quickly**
  - New Placement Reuse Flow speeds time to market by solving performance issues due to last-minute ECOs or changes in functional requirements
  - *PreciseTime* allows "what-if" and incremental timing analysis
  - Automated physical synthesis improves performance and reduces the runtime of subsequent P&R iterations
- **Meet Project Requirements**
  - New Divide and Conquer Flow saves time by targeting optimization to the design portions that need it most
  - *PreciseView*, the placement and timing debug editor, reduces costs and increases performance
  - Cross-probing between RTL, schematic, timing, and physical views of the design enhances analysis



*Precision Synthesis enables high-productivity FPGA design flows.*

requirements. But getting started right also means getting started quickly and easily. Precision Synthesis offers broad language support including the industry's most complete implementation of Verilog 2001 today. The tool supports a full range of FPGA devices and platforms.

**Intelligent Optimization:** A suite of unique algorithms automatically focuses specific optimizations on design areas most likely to be performance bottlenecks, such as finite state machines, cross-hierarchical logic, and paths with excessive combinational logic. An automated, heuristic approach delivers smaller, faster designs with the first pass.

**Optimizations Across Boundaries:** Advanced optimization technology overcomes performance-limiting barriers, including register, hierarchy and operator boundaries. The powerful re-timing algorithm balances logic across register boundaries, hierarchy optimization minimizes logic between modules, and pipelining inserts registers into multipliers. Precision Synthesis identifies when and where to employ these algorithms, easily improving performance by up to 70 percent.

**FSM Optimization:** Finite state machines are automatically detected and optimized. Various encoding styles are then evaluated to determine the best implementation for your design and target technology.

**Advanced Technology Inferencing:** The latest FPGA devices include embedded components that

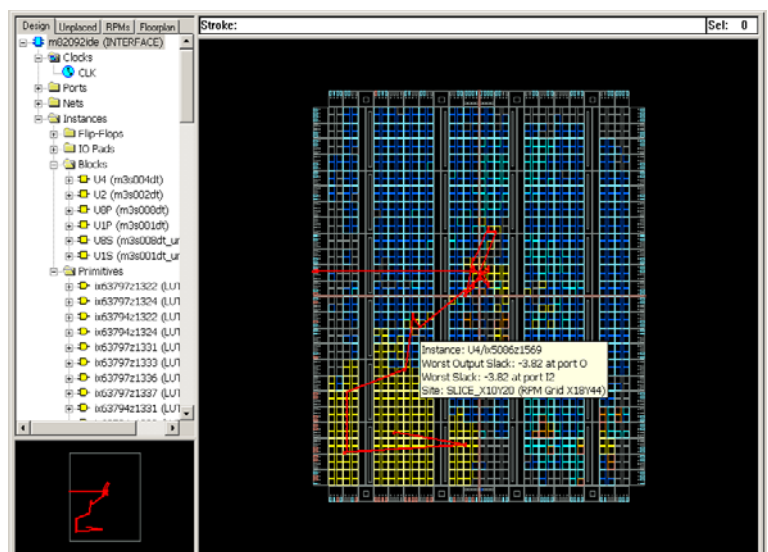
– when used appropriately—enable superior performance. But manually putting these elements into designs is a cumbersome process and creates technology dependencies in your source code. Precision Synthesis automatically infers key technology components like memories and DSP structures to keep your code clean and transportable.

## Improve Designs Quickly and Efficiently

Precision Synthesis enhances and augments traditional RTL synthesis functionality with physically aware algorithms:

**Placement Optimization,** as the primary approach to physical synthesis, automatically moves cells contained within critical timing paths close together. The advanced physically aware interconnect delay estimation algorithm in Precision Synthesis ensures that placement optimizations produce superior and predictable results.

**Retiming** moves registers in a synchronous circuit to balance the register-to-register delay. Often accompanied by register replication, retiming works favorably with an FPGA's register-rich architecture. With accurate knowledge of the placement and interconnect delay values, Precision Synthesis can optimally relocate the resources of the retimed circuit.



*Cells are colored based on slack, critical timing paths and detailed timing data to help you improve design performance.*

**Register Replication** benefits from the ability to control placement of replicated registers. Registers that fan out to different areas of the design are optimized by placing individual registers in each region. This further improves on the typical approach, which replicates solely based on fan-out requirements. Delay estimates are calculated using knowledge of the device architecture and available routing resources, enabling Precision Synthesis to make accurate calculations of the new net delays.

**Re-synthesis** restructures logic based on physical requirements. Often, an optimal implementation of a logical structure becomes inefficient after a place-and-route run. With Precision Synthesis, timing-critical logic is optimally restructured by using knowledge of device topology.

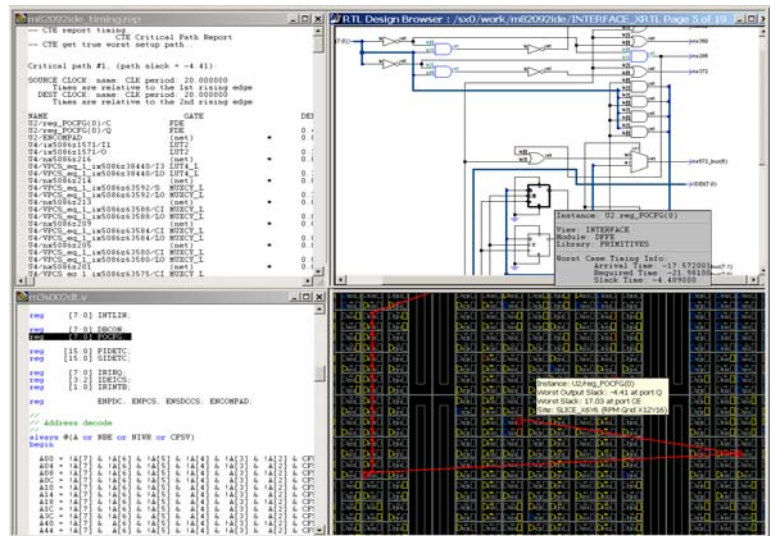
**Interactive Timing Analysis:** The information you receive about device timing should not be limited to a few pre-selected paths in a synthesis report. A design team's skill and experience is fully utilized with visibility into the implementation of the design. Precision Synthesis has a built-in set of powerful analysis features called *PreciseTime* that give you the information needed to make important tradeoffs. Interactive timing analysis quickly generates detailed timing reports from any port, pin, or instance. Timing queries can be initiated throughout the user interface, including selected objects in the schematic viewer.

## Expert Control to Meet Every Challenge

Precision Synthesis offers a powerful analysis and debug environment to help you deliver on your design goals.

**Schematic Viewing:** An integrated schematic viewer provides a clear visualization of the design and of the synthesis process. High-level RTL schematics help you determine the impact of coding styles, while detailed technology schematics show where and how device-specific resources (such as RAM and DSP blocks) are utilized. Precision Synthesis offers patented path viewing and filtering technology to display concise fragments of timing-critical logic.

**Interactive Editing:** In cases where additional performance is desired, or for users who want to tailor their results for specific purposes, Precision Synthesis includes an interactive layout editor and physical implementation diagnostic tool called *PreciseView*. This tool is ideal for the advanced user,



*Cross-probing gives you the visibility to trace from the physical implementation to the original line in the RTL source code that relates to any potential problem.*

and it now also includes new features and options that make it more accessible to the less experienced user. Since timing information is readily available, you can easily spot trouble areas and clearly understand how to address these problems. Edits are checked for legal placements in real time. This “correct-by-construction” approach makes it impossible to create a design rule violation. Finally, the tight integration with different views of the design, be it the original RTL source or the mapped logical design, easily determines how a particular physical implementation occurred and how it may be modified.

**Cross-probing:** Precision Synthesis offers comprehensive cross-probing capabilities from any element in any report to either the design schematic or the physical layout in *PreciseView*. You can cross-probe from the timing path reports provided by both Xilinx and Altera to the same timing reports in Precision Synthesis. Cross-probing is available from a placed cell in *PreciseView* to the RTL source file, or to the schematic. Cross-referencing is also available from physical location names, often seen in P&R reports, to any view in Precision Synthesis. With each step in the design flow impacting names (either changing existing names or adding new objects with new names), you will find that robust cross-probing is absolutely necessary for efficient design completion.

**Constraint Analysis:** Missing timing constraints result in incomplete timing analysis and may allow errors to go undetected until board debug. Precision Synthesis eliminates this

unnecessary risk by performing a complete constraint analysis prior to synthesis, ensuring that designs are fully and accurately constrained.

## Powerful Reuse/Optimization Flows

Traditional FPGA design approaches are often inadequate, as larger, complex designs demand more efficient ways to tackle new challenges. Precision Synthesis offers three innovative flows to solve these challenges.

**Modular Design Flow:** Companies are increasingly turning to block-level reuse to leverage their technology across projects and platforms. In FPGAs, reuse at the RTL stage is good, but it is not enough for high-performance designs. Precision Synthesis now supports a modular design flow that enables component technology to be designed once and then used multiple times within a design or across projects. This can significantly reduce time to market and project risk.

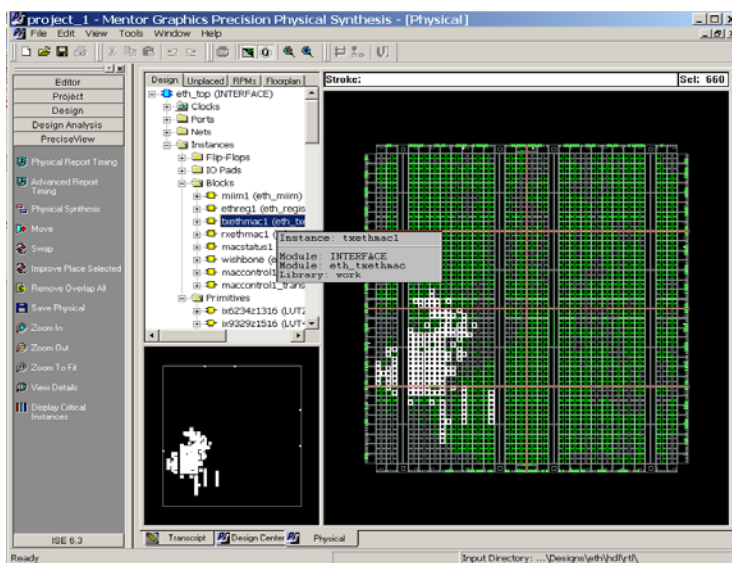
**Placement Reuse/ECO Flow:** When market demands force last-minute design modifications, “pushbutton” synthesis can put the whole design project at risk. The placement reuse/ECO flow overlays placements at the gate level, such that only the logic affected by the changes is re-placed. This new flow uses sophisticated placement and timing-driven “nudging” algorithms for optimal results. With this flow, completed sections of the design that have previously met timing goals remain untouched, thus assuring the shortest path to new functionality.

**Divide and Conquer Flow:** Timing closure continues to demand more engineering time and effort, while

increasing risk. The “divide and conquer” flow protects areas that are already working by “locking down” placement of the design outside of the performance-critical blocks. Design expertise is then focused on improving the performance-critical sections. This easy-to-use flow can substantially improve FPGA design productivity.

## Supported Technologies and Platforms

Precision Synthesis runs on Windows, Linux and Solaris, and supports a broad range of devices from Actel, Altera, Atmel, Lattice Semiconductor, Xilinx and other vendors. New devices, vendors and platforms are frequently being added.



*The Divide and Conquer Flow enables you to easily extract blocks as macros to allow isolated optimization.*

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